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Implementation of Full adder Using CMOS Logic Styles Based On Double Gate MOSFET

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Abstract----CMOS transistors are widely used in designing digital circuits. Transistor level design is an important aspect in any digital circuit designs essentially full adders. Full adder is the basic component in any of the arithmetic circuits and its applications include micro-processors, micro controllers, digital signal processing ICs etc. Scaling down the transistor sizes below 50nm lead to several disadvantages such as short channel effects, drain induced barrier leakage, variation in threshold voltage etc. These demerits are overcome by using double gate Mosfets. Also performance of double gate MOSFET is found to be better than single gate devices in terms of power and delay. In this paper, Pass transistor logic styles are implemented using double gate MOSFET and power characteristics has been compared and analyzed using HSPICE under varying conditions of capacitances and frequency.

Index terms---double gate MOSFET, HSPICE, PTM 32 nm, Complementary Pass Transistor Logic(CPL), double pass transistor logic(DPL),degenerative pass transistor logic(DGPL)

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1 INTRODUCTION

Double gate MOSFET was proposed in the year 1980s. According to the technology trends from International technology roadmap for semiconductors (ITRS), the millions of transistors per chip is on the surge every year. Moore's law states that the number of transistors on integrated circuits doubles approximately every two years. The 2010 update of International technology roadmap for semiconductors predicts that the growth will slow at the end of 2013, when transistor counts are to double only every three years. It also predicts that the physical gate length would reach 11.7nm by the year 2018.This suggests that transistors size are likely to reduce in the future. When transistors are scaled down in the below 50nm gate length, it leads to drawbacks such as short channel effects, increased leakage current, decrease in threshold voltage etc. These drawbacks are overcome by using double gate transistors. Hence, when scaling down transistors below 50nm gate length, double gate transistors are highly preferred[1].

There are various models of double gate MOSFET. They are planar structure, non-planar structure and finfet.Finfet is found to be the most promising technlogy. Hence it is chosen in this paper. Full adders are designed using various CMOS logic styles. Each CMOS logic style has its own advantage in terms of power, delay and area. Thus transistor logic styles are implemented using double gate MOSFET [1].

2 DOUBLE GATE MOSFET

2.1 PHYSICAL STRUCTURE

As the devices scale down in nano scale regime alternative device structures are required. Double gate transistor was proposed in the year 1980s.Double gate transistor comprises of a conducting channel which is surrounded by top and bottom gate electrodes. No part of the channel is far from the gate electrodes. The voltage applied on the gate electrodes controls the amount of current flow through the channel. The common mode of operation is the shorted gate mode where both the gates switch at the same time. The second mode of operation is applying bias to the back gate and to switch only one gate[1].

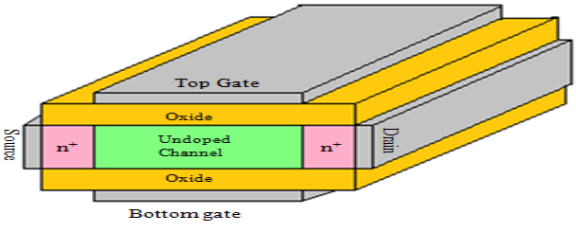

Fig 1: Double gate MOSFET structure

2.2 ADVANTAGES OF DOUBLE GATE MOSFET

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Short channel effects (SCE) are reduced. For small lengths of channel, SCE lowers the threshold voltage which increases the leakage current. Use of double gate MOSFET reduces the short channel effects. Current drive capability is improved through double gate MOSFET. Impurity scattering is minimized and intrinsic parameter fluctuations are eliminated through the use of undoped channel [1].

3 CMOS LOGIC STYLES

3.1 COMPLEMENTARY PASS TRANSISTOR LOGIC

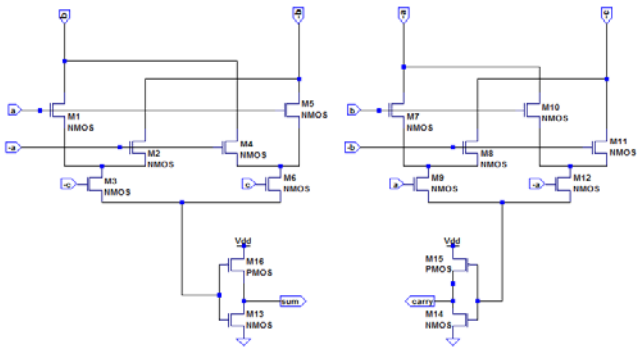

Fig 2: Complementary pass transistor logic

Complementary pass transistor logic has only nmos transistors. In pass transistor logic the input signals are directly given to the source of the transistors and supply voltage is not used. A weak pMOSFET feedback device can also be added at the output end in order to pull the pass transistor outputs to full supply voltage level. This may lead to increase in the output node capacitance which increases the power dissipation and the propagation delay. Complementary input signals are required to generate both sum and carry [2]

3.2 DOUBLE PASS TRANSISTOR LOGIC

Fig 3: Double pass transistor logic

It has both PMOS and NMOS transistors to achieve full swing . It is implemented using double gate MOSFET in SG mode. It can operate in low voltages with better speed performance than CPL. It is a 28 transistor model. The addition of PMOSFETs leads to increased input capacitances [2]

3.3DEGENERATIVE PASS TRANSISTOR LOGIC

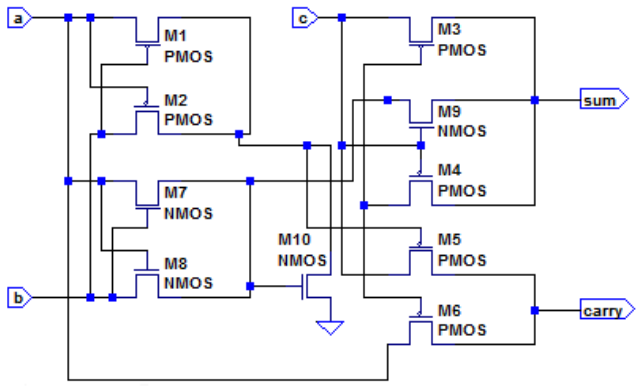

Fig 4: Degenerative pass transistor logic

It is a 10 transistor model. A 5 transistor XOR-XNOR module is used to generate the complementary signals. These complementary control signals are given to the circuits to generate the sum and carry. They also allow the selection of sum and carry modules and avoid the multi- threshold loss problems.

3.4POWER CHARACTERISTICS IN DOUBLE GATE MOSFET FULL ADDERS

Power in CMOS circuits can be classified as static power dissipation, dynamic power dissipation and short circuit power dissipation. As the leakage current is reduced in double gate MOSFET static power dissipation is reduced to a great extent when compared to single gate MOSFETs. The dynamic power dissipation depends on three factors. They are supply voltage, load capacitance and frequency [2]

$$Pd=CL\ Vdd2\ f$$

The dynamic power consumption increases with the increase in load capacitance, supply voltage and frequency. In this paper, by varying the factors such as load capacitance and frequency the power characteristics of double gate MOSFET circuits are measured [2].

4 PROPOSED SYSTEM

The three pass transistor logic styles are implemented using double gate MOSFET and their power characteristics are compared.

4.1COMPLEMENTARY PASS TRANSISTOR LOGIC

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Fig 5: Complementary Pass transistor logic in double gate MOSFET

4.2DOUBLE PASS TRANSISTOR LOGIC

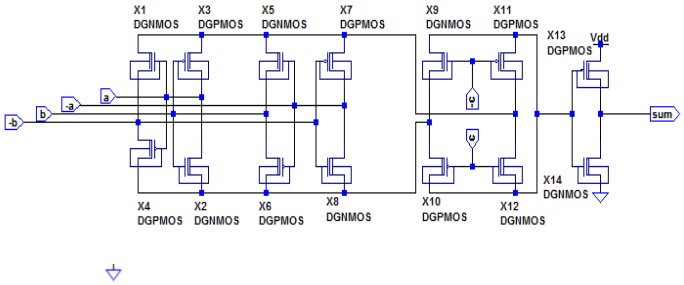

Fig 6: Double pass transistor logic in double gate MOSFET

4.3DEGENERATIVE PASS TRANSISTOR LOGIC

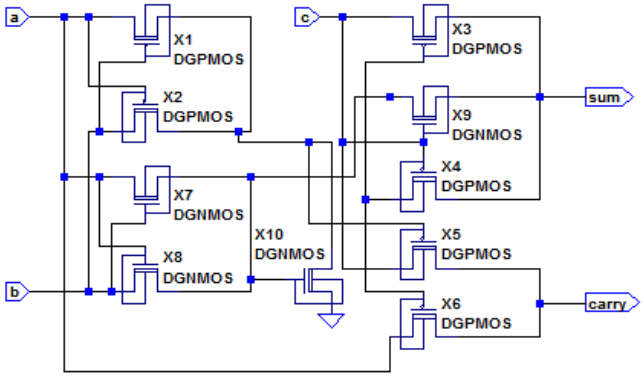

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Fig 7: Degenerative pass transistor logic in double gate MOSFET

5 SIMULATION RESULTS AND ANALYSIS

PTM 32nm Finfet model is used to implement the adder circuits with double gate MOSFET. The simulation is done using HSPICE.

The load capacitances are varied from 2PF to 10PF with VDD=0.4v, f=1MHZ and the power characteristics of three pass transistor logic styles are compared. For all values of capacitances the power is lower for degenerative pass transistor logic full adder. Among the other two logics, CPL and DPL, for values of capacitance of 2PF the power is lower for double pass transistor logic and for the values of capacitances from 4PF to 10PF complementary pass transistor logic performs well when compared to double pass transistor logic.

For various values of frequency the power characteristics of three pass transistor logic styles are compared at VDD=0.4v, CL=1PF. At all frequencies degenerative pass transistor logic performs better than other logics. Of the two logics CPL and DPL, at lower frequency of 0.1MHZ complementary pass transistor logic is better logic and at frequency of 1MHZ double pass transistor logic is better, at a frequency of 10MHZ complementary pass transistor logic is a better logic.

5.1 SIMULATION RESULTS

COMPLEMENTARY PASS TRANSISTOR LOGIC

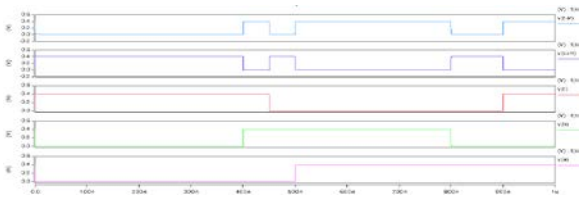

Fig 8: Complementary pass transistor logic simulation result

DOUBLE PASS TRANSISTOR LOGIC

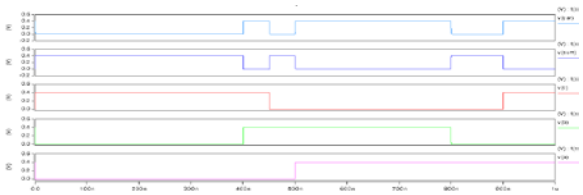

Fig 9: Double pass transistor logic simulation result

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DEGENERATIVE PASS TRANSISTOR LOGIC

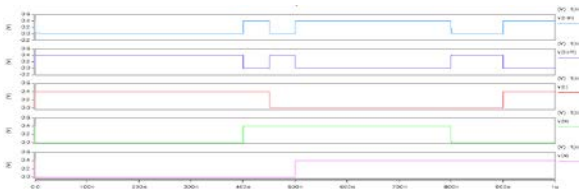

Fig 10: Degenerative pass transistor logic simulation result

TABLE 1: POWER CHARACTERISTICS WITH VARYING CL, VDD=0.4V, F=1MHZ

CL (PF)	CPL Power(μw)	DPL Power(μw)	Degenerative pass logic power(μw)
2	1.9375	1.8819	1.6264
4	3.6074	3.6335	2.9758
6	5.0443	5.0755	4.1762
8	6.3138	6.3609	5.2740
10	7.4651	7.6504	6.2153

Fig 11:Power Vs CL

TABLE 2: POWER CHARACTERISTICS WITH VARYING FREQUENCY, VDD=0.4V,CL=1PF

f(MHZ)	CPL Power(μw)	DPL Power(μw)	Degenerative pass logic(μw)
0.1	0.1663	0.1820	0.1528
1	1.0061	0.9750	0.8383
10	6.6813	7.1391	5.3172

Fig 9: Power Vs Frequency

6 CONCLUSIONS AND FUTURE WORK:

From the results we observe that degenerative pass transistor logic is better among the three logics. Among the two logics, CPL and DPL Complementary pass transistor logic is better for values of higher load capacitances and double pass transistor logic is better for lower value of load capacitances. Complementary pass transistor logic is preferred for higher and lower values of frequencies. Double pass transistor logic is better for values of

mid-range of frequencies. Under conditions of lower capacitance and lower frequency double pass transistor logic is better of the two logic styles.

The analysis could be extended to different logic styles and under different conditions.

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